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Streaming Multi-port SDRAM User Manual

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Streaming Multi-port SDRAM User Manual The Microtronix Avalon Multi-Port SDRAM Memory Controller IP Core is designed for building low latency Avalon-MM-based, multi-master streaming data systems Its advanced design features enable maximum system clock rates using low-speed FPGAs and standard memory devices Avalon Multi-Port SDRAM Memory

M AVALON MULTI PORT ONTROLLER

Avalon Multi-port SDRAM Controller Page 9 of 39 Local Ports The SDRAM memory controller has up to sixteen Avalon local ports Each port has an internal FIFO, which acts as a bridge between the local interface and the SDRAM memory Each port can be configured as an Avalon Random Slave, or an Avalon Burst Slave

HyperDrive Multi-Port DDR2 Memory Controller

HyperDrive Multiport DDR2 SDRAM User Manual Transfers are not limited to the size of the internal FIFO After the initial prefetch, the read port will fetch data from the SDRAM as needed in blocks of half the FIFO size The BUSY signal is asserted when data is no longer available in the FIFO

Once more data is read from the

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AVALON MULTI-PORT SDRAM MEMORY CONTROLLER IP CORE The Microtronix Avalon Multi-port SDRAM Memory Controller IP Core is required to interface to the on-board DDR2 SDRAM devices It is designed to maximize the performance of the Altera Nios II processor in Avalon® multi-master streaming data systems

Avalon Mobile DDR Memory Controller

When a port is active, and another port requests access to the memory the first port can only retain access to the SDRAM up to the maximum number of words specified for the FIFO depth or the burst length By this means, each port is assured access to the SDRAM memory system

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